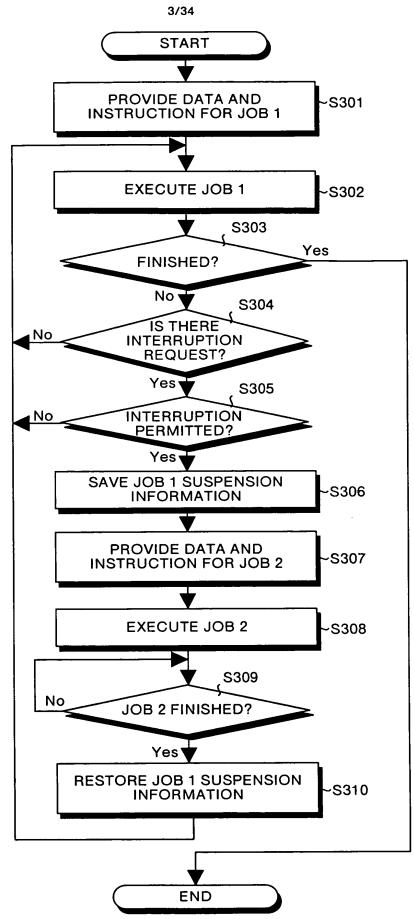


TARREST WATER

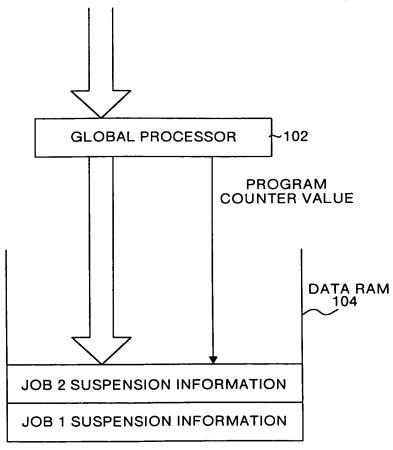
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FROM SIMD TYPE ARITHMETIC PROCESSING SECTION 101 (CONTENTS OF ACCUMULATOR, REGISTER, DATA REGISTER)





TO SIMD TYPE ARITHMETIC PROCESSING SECTION 101
(CONTENTS OF ACCUMULATOR, REGISTER, DATA REGISTER)

GLOBAL PROCESSOR

PROGRAM
COUNTER VALUE

JOB 2 SUSPENSION INFORMATION

DATA RAM
104

FIG.6

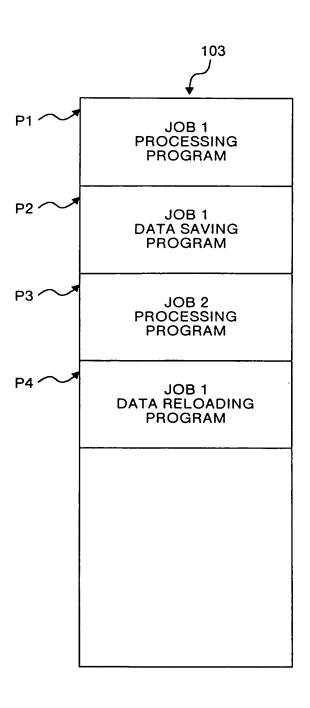


FIG.7A

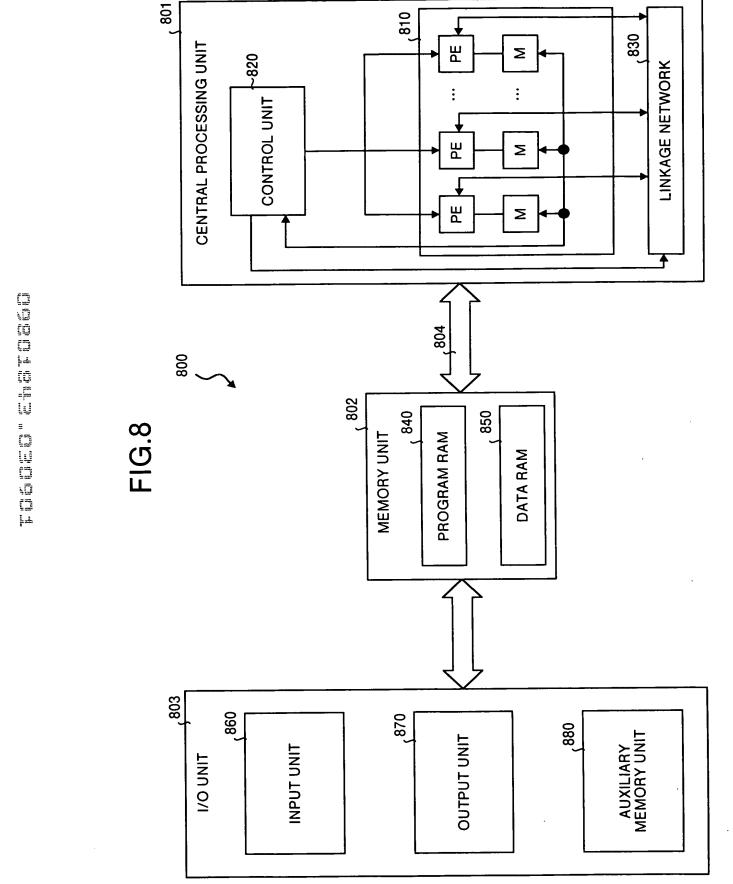
			104
PARAMETER DATA FOR PROGRAMMING JOB 1	PARAMETER DATA FOR PROGRAMMING JOB 2	EMPTY AREA	

## FIG.7B

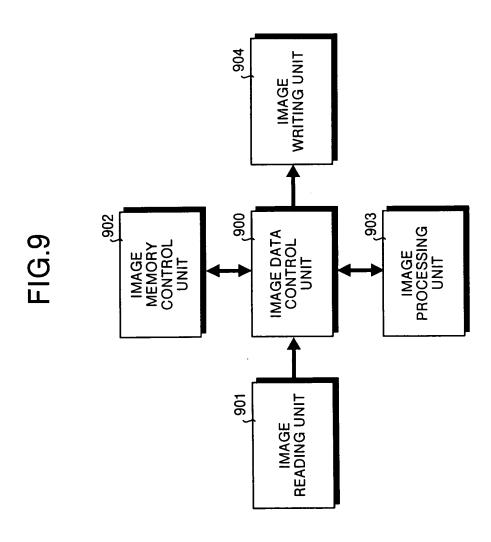
PARAMETER DATA FOR DATA FOR PROGRAMMIN G JOB 1

EMPTY AREA

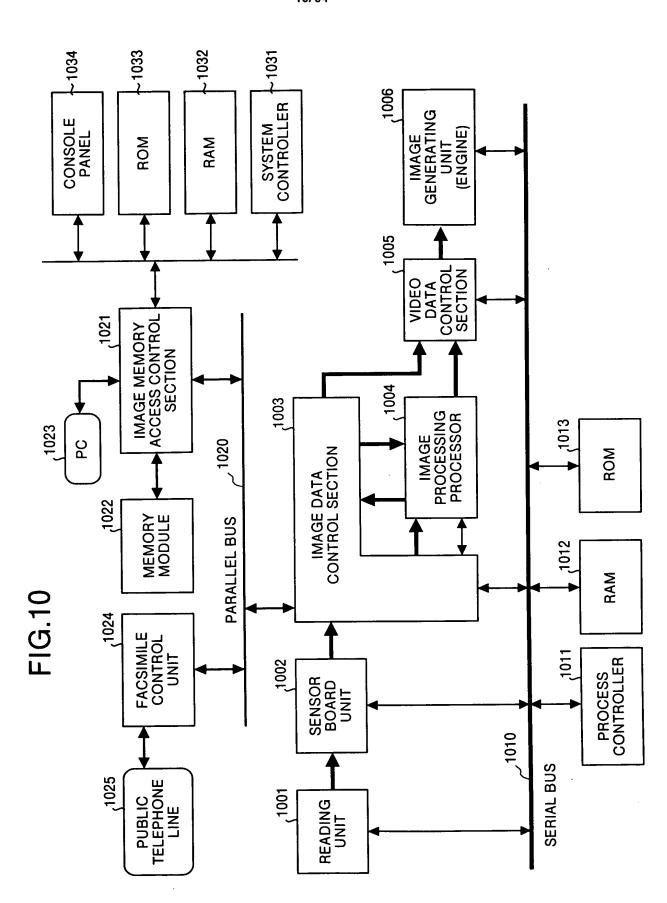
EMPTY AREA

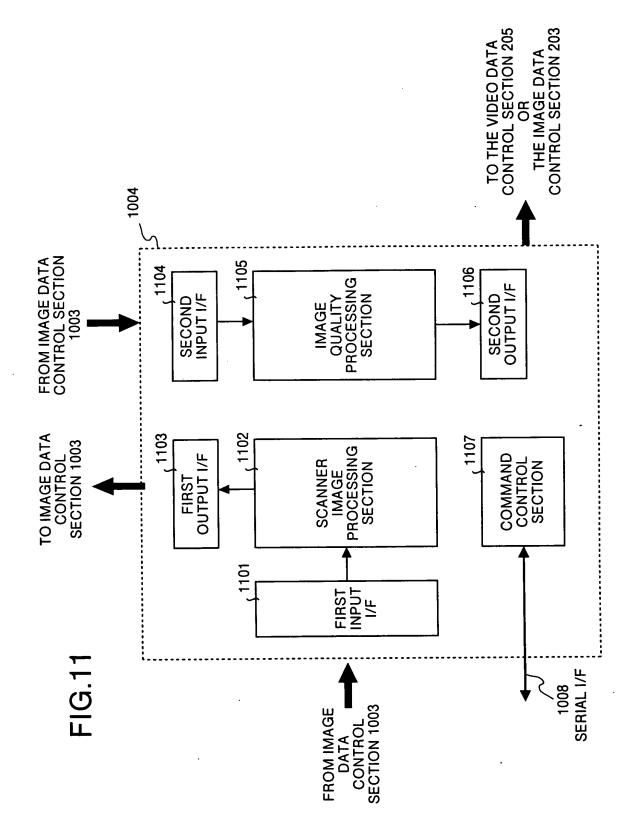








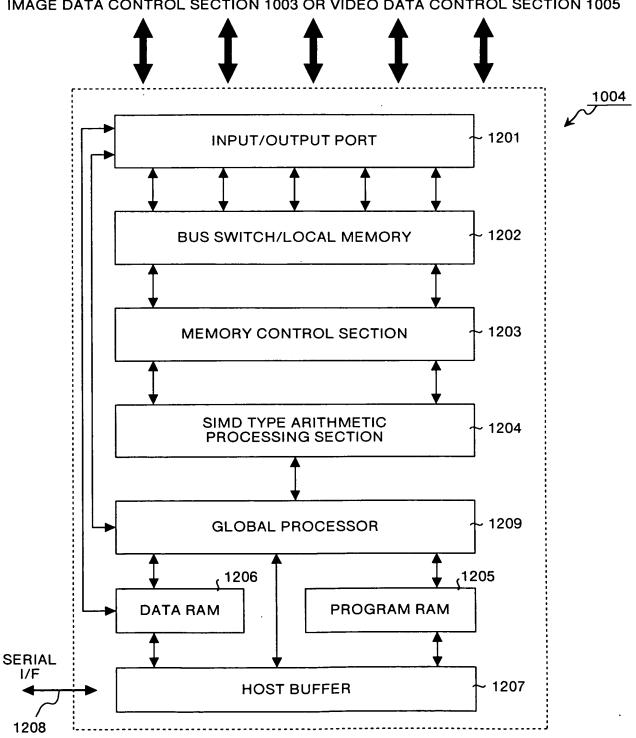






## **FIG.12**

IMAGE DATA CONTROL SECTION 1003 OR VIDEO DATA CONTROL SECTION 1005



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,1202 RAM RAM RAM RAM RAM RAM  $\sim 1207$ → SERIAL I/F INTERRUPTION NUMBER 1203 MEMORY SWITCH (1205 DATA RAM GLOBAL PROCESSOR PPROGRAM RAM MEMORY CONTROLLER R16 CONTROLLER R15 CONTROLLER R17 CONTROLLER R18 CONTROLLER MEMORY CONTROLLER (1209 RAM12

RAM13

RAM13

SWITCH

RAM14

SUPERIMPOSITION DATA,

RAM14

SUPERIMPOSITION DATA,

THINNING/
RAM14

SUPERIMPOSITION DATA,

THINNING/
RAM14

SUPERIMPOSITION DATA,

THINNING/
SUPERIMPOSITION DATA,

THINNING/
SUPERIMPOSITION DATA,

THINNING/
SUPERIMPOSITION DATA,

SUPERIM HOST BUFFER R14 R19 1204) HMEMORY MEMORY CONTROLLER BH R6
SWITCH MEMORY CONTROLLER BH R7 MEMORY CONTROLLER BARD **₩EMORY CONTROLLER B**HR2 MEMORY CONTROLLER BINRS MEMORY CONTROLLER B R4 MEMORY CONTROLLER BINE MEMORY CONTROLLER BMR8 MEMORY CONTROLLER BINRS MEMORY CONTROLLER BI€ R1 (1206 1203 MEMORY SWITCH RAM SWITCH! BUS SWITCH SWITCH 3 1202 CONTROL COUTPUT BUS 2 CONTROL COUTPUT BUS 0 DATA INPUT/ OUTPUT BUS 3 DATA INPUT/ OUTPUT BUS 4 CONTROL COUTPUT BUS 1 DATA RAM BUS 1201 DATA CONTROL \*\* CONTROL \*\* DATA DATA CONTROL # SIGNAL

8Bit Reg

8Bit Reg 8Bit Reg

7to1MUX Shift Expand 16bALU ⋖ ட 8Bit Reg 8Bit Reg 8Bit Reg 8Bit Reg 7to1MUX Shift Expand 16bALU ⋖ щ 8Bit Reg 8Bit Reg 8Bit Reg 8Bit Reg 7to1MUX Shift Expand 16bALU ⋖ ш 8Bit Reg 8Bit Reg 8Bit Reg 8Bit Reg 7to1MUX Shift Expand 16bALU ⋖ ட FIG.14 8Bit Reg 8Bit Reg 8Bit Reg 8Bit Reg 7to1MUX Shift Expand 16bALU Þ щ 8Bit Reg 8Bit Reg 8Bit Reg 8Bit Reg 7to1MUX Shift Expand 16bALU ⋖ ட 8Bit Reg 8Bit Reg 8Bit Reg 8Bit Reg 7to1MUX Shift Expand 16bALU/ ш ⋖ ADDRESS BUS, DATA BUS 8Bit Reg 8Bit Reg 8Bit Reg 8Bit Reg 7to1MUX Shift Expand 16bALU ⋖ ш 8Bit Reg 8Bit Reg 8Bit Reg 8Bit Reg 1406-1403-1405 1402 1404 1401

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8Bit Reg OBLON, SPIVAK, ET AL DOCKET #:203930US6
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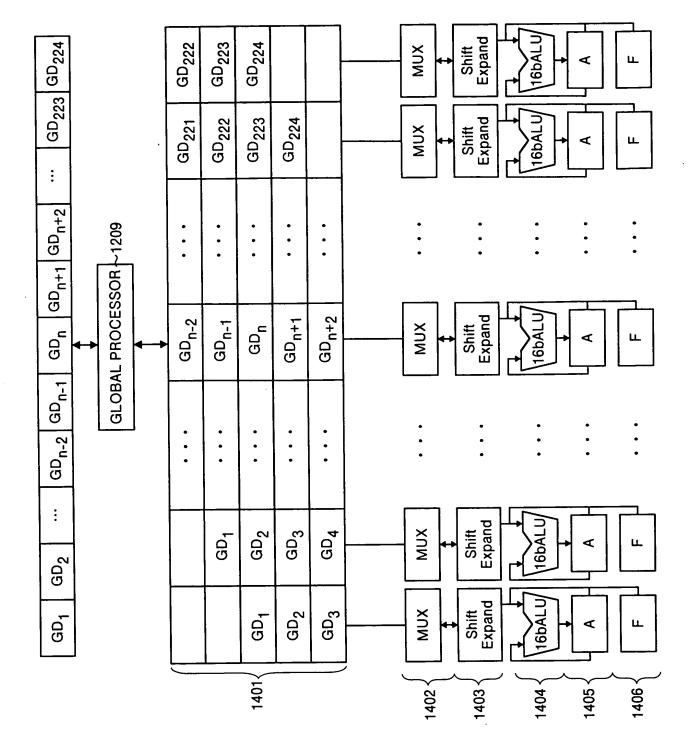
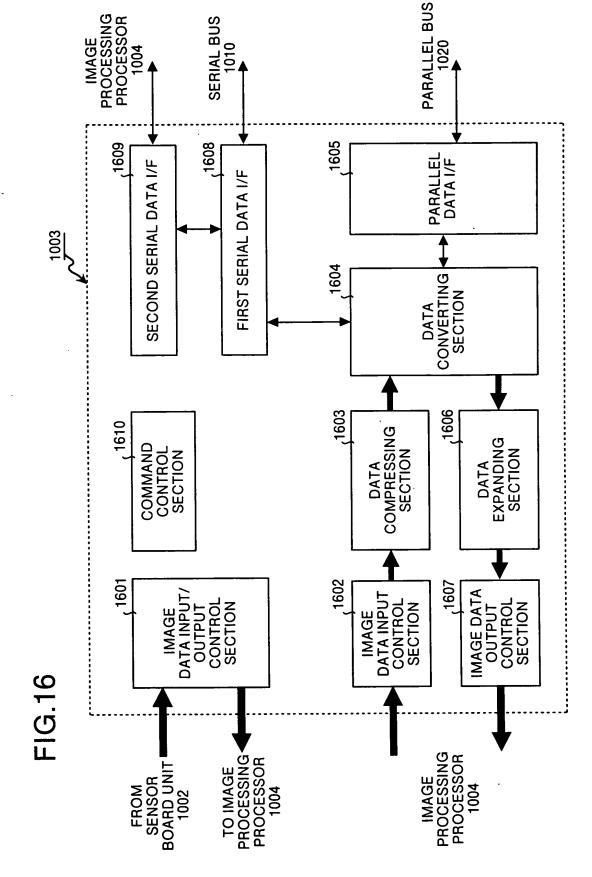


FIG.15



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TO IMAGE FORMATION UNIT 1006 SERIAL BUS 1010 SERIAL DATA I/F , 1702 PULSE CONTROL SECTION 1705 DATA CONVERTING SECTION EDGE SMOOTHING SECTION 1703 PARALLEL DATA I/F FROM IMAGE
PROCESSING
PROCESSOR 1004
OR
IMAGE DATA
CONTROL
SECTION 1003 PARALLEL BUS 1020

FIG.17

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PARALLEL BUS 1020 1801 PARALLEL DATA I/F 1021 1808 DATA CONVERTING SECTION ~ 1804 1806 1807 1805 DATA COMPRESSING SECTION DATA EXPANDING SECTION **FROM PC1023 LINE BUFFER** VIDEO CONTROL SECTION 1802 1803 SYSTEM CONTROLLER 1/F MEMORY ACCESS CONTROL SECTION SYSTEM CONTROLLER▲ 1031 MEMORY MODULE 1022

FIG. 18

FIG.19

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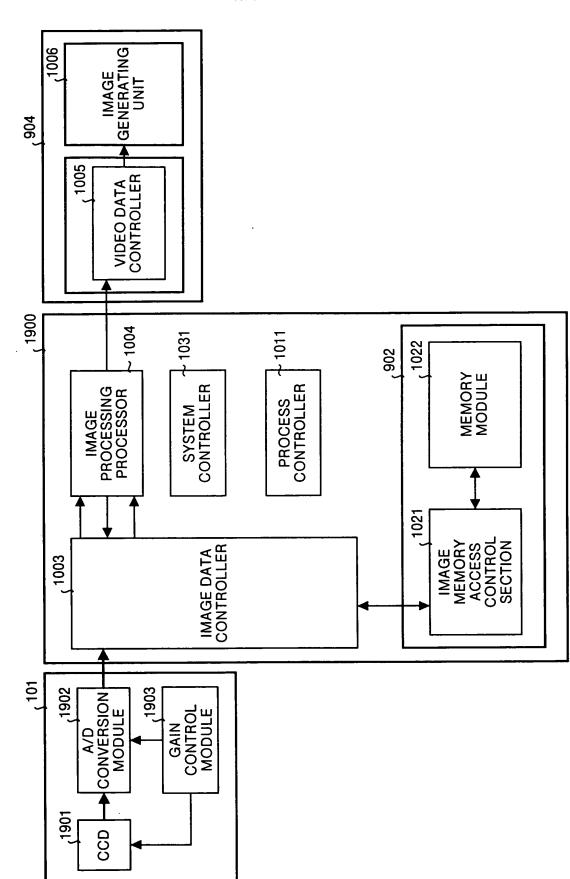




FIG.20

	j-2	j-1 (	COLUMN j+1		j+2
i-2	Α	В	С	D	E
i-1	F	G	Н	_	J
ROW i	К	L	М	Z	0
i+1	Р	Q	R	S	Т
i+2	U	V	W	×	Y

FIG 2

	٦ ،			
		-		
S		ď		C
	_			
			i i	
				<u> </u>
DATA		DATA		; DATA

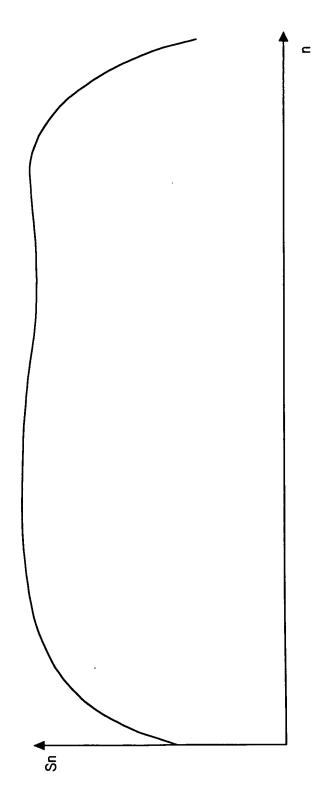
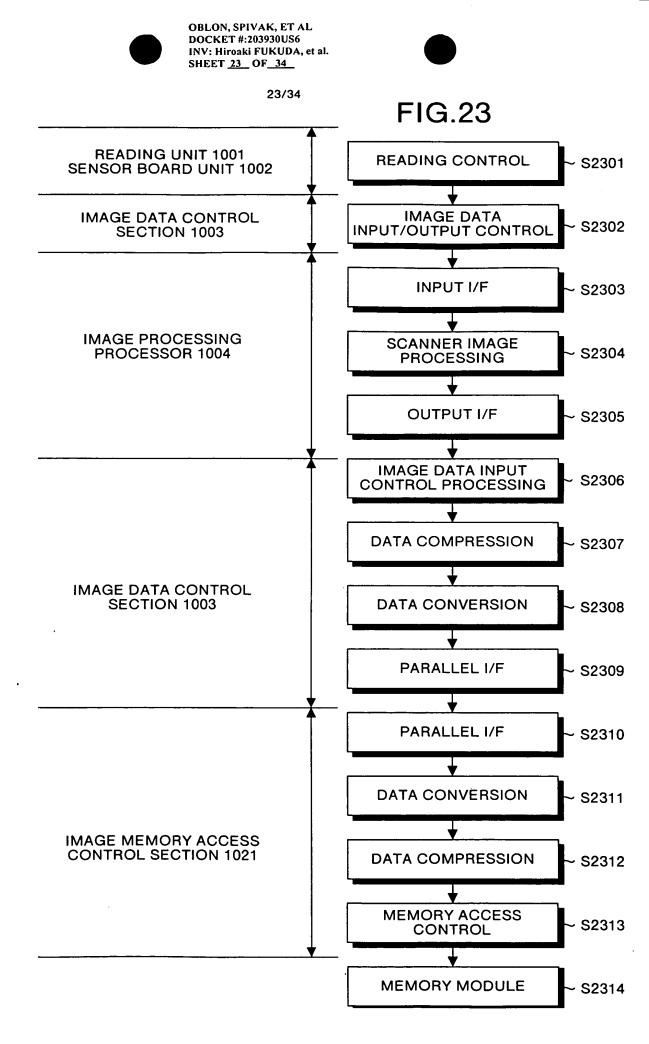
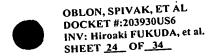
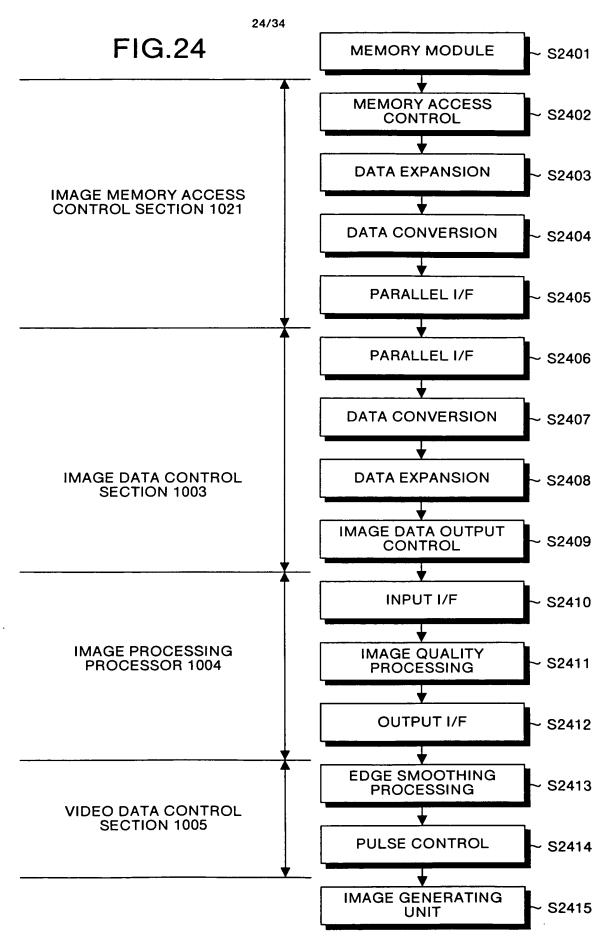
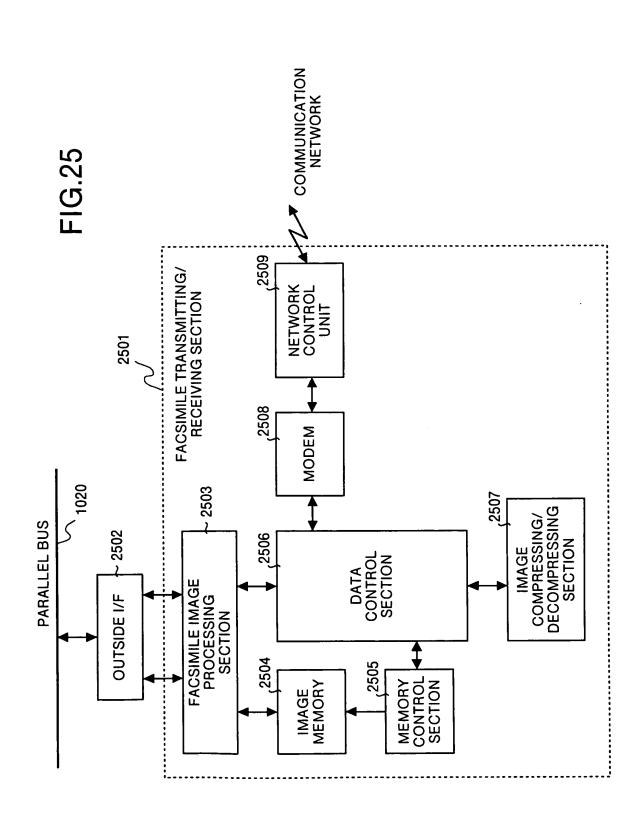


FIG.22

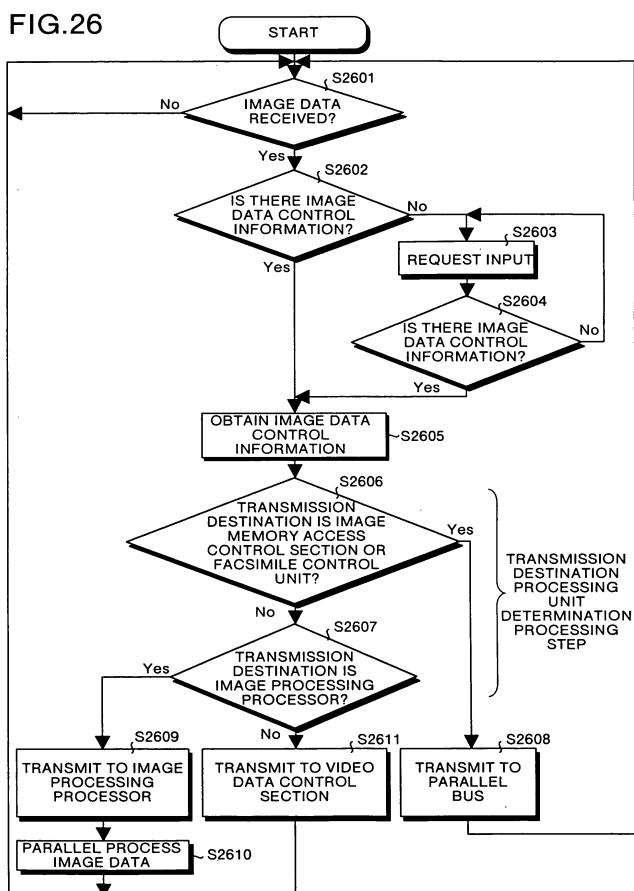


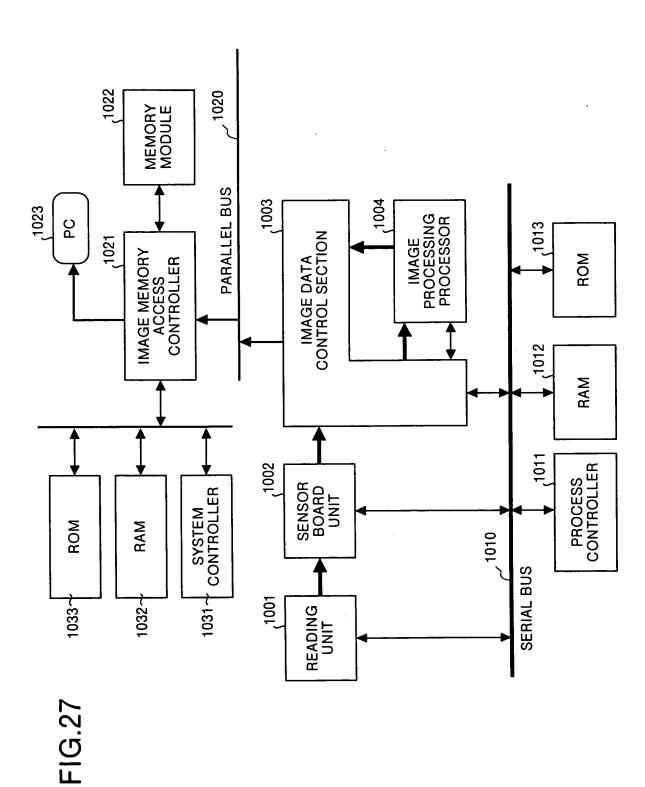




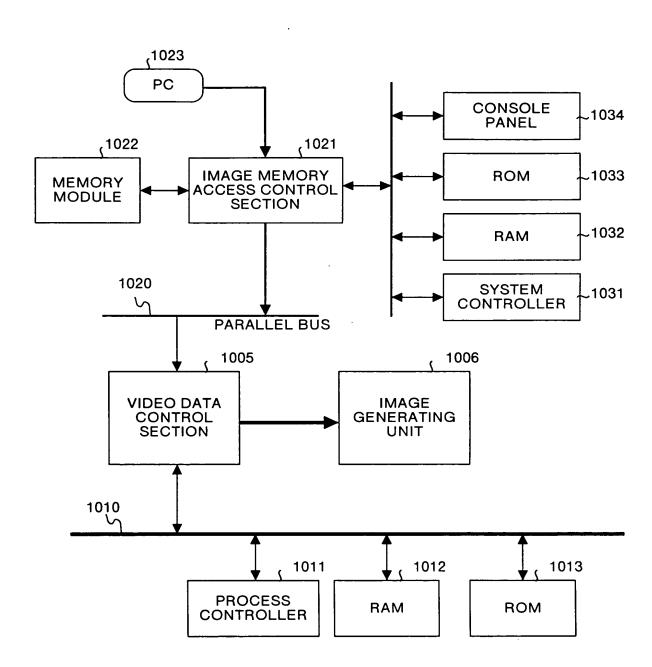


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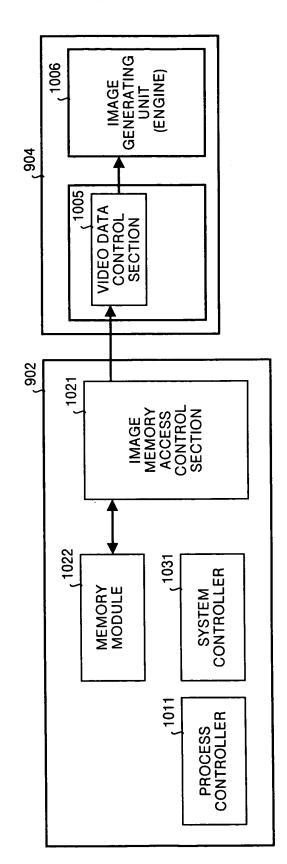




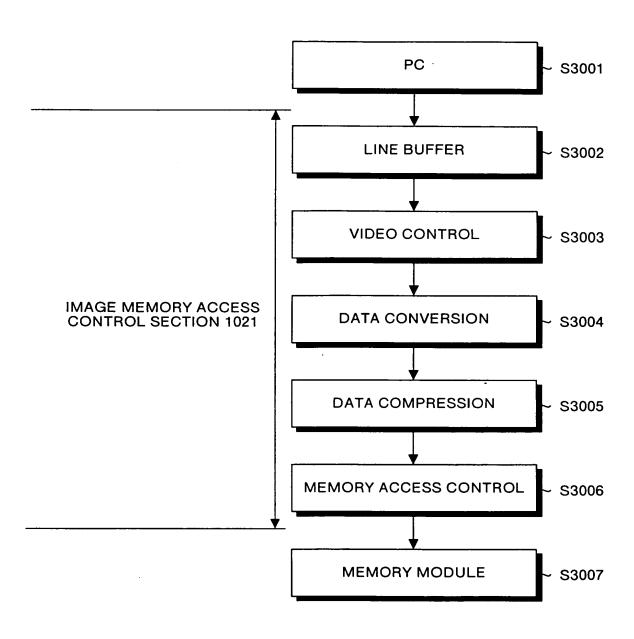




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**FIG.30** 



**FIG.31** 

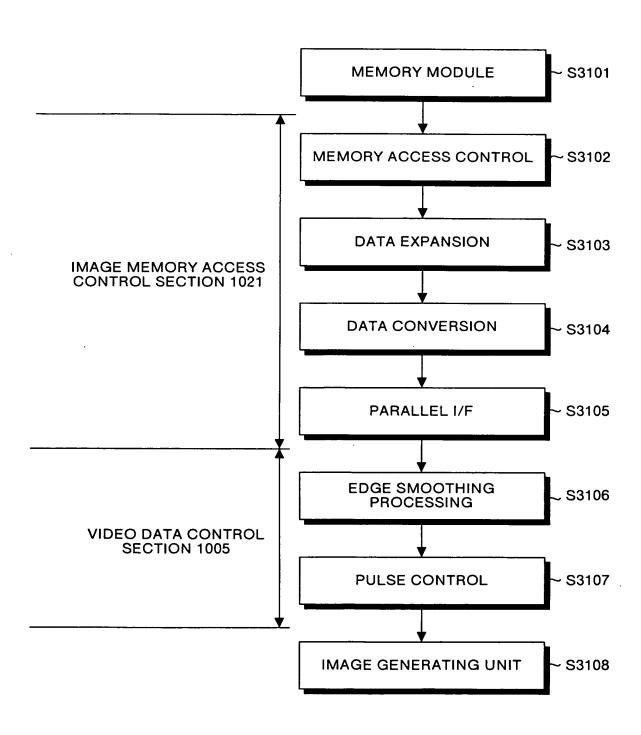
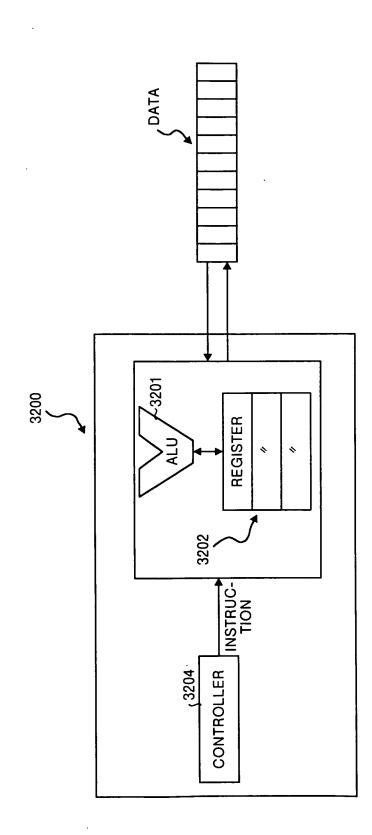
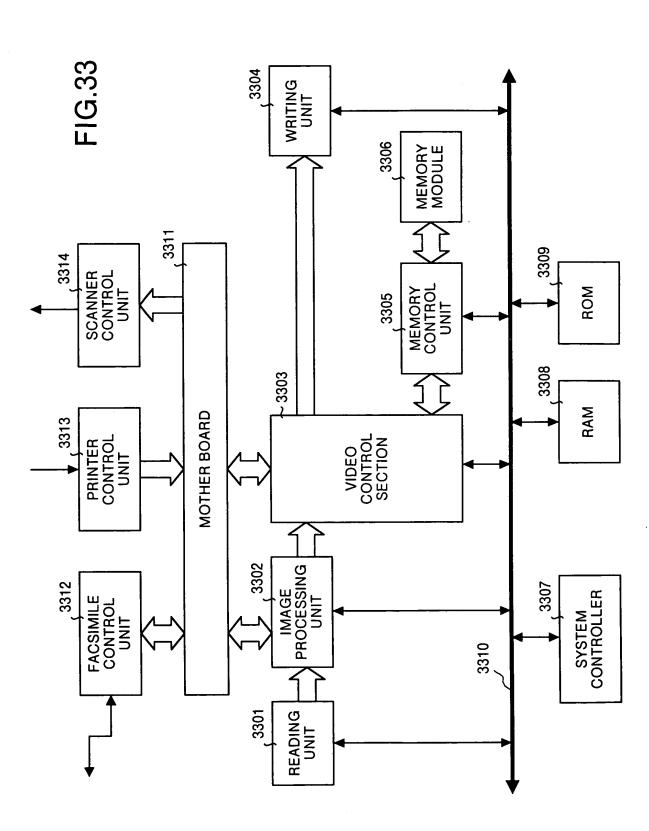


FIG.32

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## **FIG.34**

